What is claimed is:

1. A production method of a semiconductor integrated circuit device having: a memory cell composed of a memory cell selecting n channel MISFET and a capacitor which are formed in a memory cell forming area of a semiconductor substrate; and an n channel MISFET and a p channel MISFET which are formed in a peripheral circuit forming area, said production method comprising:

(a) a step of forming a gate insulating film on said semiconductor substrate;

(b) a gate electrode forming step of forming a silicon film and an insulating film on said gate insulating film, and forming, by patterning, gate electrodes of a memory cell selecting n channel MISFET, an n channel MISFET, and a p channel MISFET and insulating films on the upper portions thereof, wherein said gate electrode forming step comprises the steps of: introducing a p type impurity into a silicon film constituting the gate electrode of said memory cell selecting n channel MISFET and the gate electrode of said p channel MISFET; and introducing an n type impurity into a silicon film constituting the gate electrode of said n channel MISFET;

(c) a step of sequentially depositing a first film and a second film on said semiconductor substrate, and leaving, by performing an anisotropic etching, the first and second films on a sidewall of the gate electrode in said peripheral circuit forming area, and filling spaces

between said gate electrodes in said memory cell forming area, with said first and second films; and

(d) a step of using said first and second films as a mask to implant an impurity into both sides of each of the gate electrodes of said n channel MISFET and said p channel MISFET and thereby form a semiconductor area.

2. The production method according to claim 1, further comprising:

a step of removing said second film in the memory cell forming area and thereafter removing said first film on said semiconductor substrate; and

a step of filling, with a conductive film, a space between the gate electrodes of said memory cell selecting n channel MISFET and thereby form a contact electrode.

3. The production method according to claim 2,

wherein said contact electrode is formed by the steps of depositing said conductive film on the gate electrodes and between the gate electrodes, and polishing said conductive film on said gate electrodes until the first film on said gate electrode is exposed.

4. A production method of a semiconductor integrated circuit device having: a memory cell composed of a memory cell selecting n channel MISFET and a capacitor which are formed in a memory cell forming area of a semiconductor substrate; and an n channel MISFET and a p channel MISFET which are formed in a peripheral circuit forming area, said production method comprising:

(a) a step of forming a gate insulating film on said semiconductor substrate;

(b) a gate electrode forming step of forming a silicon film and an insulating film on said gate insulating film, and forming, by patterning, gate electrodes of a memory cell selecting n channel MISFET, an n channel MISFET, and a p channel MISFET and insulating films on the upper portions thereof, wherein said gate electrode forming step comprises the steps of: introducing a p type impurity into a silicon film constituting the gate electrode of said memory cell selecting n channel MISFET and the gate electrode of said p channel MISFET; and introducing an n type impurity into a silicon film constituting the gate electrode of said n channel MISFET;

(c) a step of using, as a mask, the gate electrode of said memory cell selecting n channel MISFET and the insulating film on the upper portion thereof to implant an impurity into the both sides of said gate electrode and thereby form a first semiconductor area in the semiconductor substrate of the memory cell forming area;

(d) a step of sequentially depositing a first film and a second film on said semiconductor substrate, and leaving, by performing an anisotropic etching, the first and second films on a sidewall of the gate electrode in said peripheral circuit forming area, and filling spaces between said gate electrodes in said memory cell forming area, with said first and second films;

(e) a step of using, as a mask, said first and second films to implant an impurity into both sides of each of the gate electrodes of said n channel MISFET and said p channel MISFET and thereby form a second semiconductor area; and

(f) a step of using, as a mask, the gate electrodes of said n channel MISFET and p channel MISFET and the insulating films on the upper portions thereof to implant an impurity into both sides of each of said gate electrodes and thereby form a third semiconductor area having a impurity concentration lower than said second semiconductor area in the semiconductor substrate of the memory cell forming area.

5. A production method of a semiconductor integrated circuit device having: a memory cell composed of a memory cell selecting n channel MISFET and a capacitor which are formed in a memory cell forming area of a semiconductor substrate; and an n channel MISFET and a p channel MISFET which are formed in a peripheral circuit forming area, said production method comprising:

(a) a step of forming a gate insulating film on said semiconductor substrate;

(b) a gate electrode forming step of forming a silicon film and an insulating film on said gate insulating film, and forming, by patterning, gate electrodes of a memory cell selecting n channel MISFET, an n channel MISFET, and a p channel MISFET and insulating films on the upper portions thereof, wherein said gate electrode forming step

comprises the steps of: introducing a p type impurity into a silicon film constituting the gate electrode of said memory cell selecting n channel MISFET and the gate electrode of said p channel MISFET; and introducing an n type impurity into a silicon film constituting the gate electrode of said n channel MISFET;

(c) a step of depositing a first film on said semiconductor substrate, and removing said first film on said semiconductor substrate in the memory cell forming area;

(d) a step of depositing a second film on said first film and said semiconductor substrate, and leaving, by performing an anisotropic etching, the first and second films on a sidewall of said gate electrode in said peripheral circuit forming area, and filling spaces between said gate electrodes in said memory cell forming area and on said semiconductor substrate, with said second film; and

(e) a step of using, as a mask, said first and second films to implant an impurity into both sides of each of the gate electrodes of said n channel MISFET and said p channel MISFET and thereby form a semiconductor area.

6. The production method according to claim 1,

wherein each of said insulating film and said first film is a film containing one of no hydrogen and little hydrogen.

7. The production method according to claim 1,

wherein said first film is a silicon oxide film and

said second film is a silicon film.

8. The production method according to claim 1,

wherein said first film is a film containing one of no hydrogen and little hydrogen, and said first and second films are films whose etching selective ratios are different.

9. The production method according to claim 1,

wherein said first film is a film containing one of no hydrogen and little hydrogen, and said first and second films are insulating films whose etching selective ratios are different.

10. A production method of a semiconductor integrated circuit device having: a memory cell composed of a memory cell selecting n channel MISFET and a capacitor which are formed in a memory cell forming area of a semiconductor substrate; and an n channel MISFET and a p channel MISFET which are formed in a peripheral circuit forming area, said production method comprising:

(a) a step of forming a gate insulating film on said semiconductor substrate;

(b) a gate electrode forming step of forming a silicon film and an insulating film on said gate insulating film, and forming, by patterning, gate electrodes of a memory cell selecting n channel MISFET, an n channel MISFET, and a p channel MISFET and insulating films on the upper portions thereof, wherein said gate electrode forming step comprises the steps of: introducing a p type impurity into

a silicon film constituting the gate electrode of said memory cell selecting n channel MISFET and the gate electrode of said p channel MISFET; and introducing an n type impurity into a silicon film constituting the gate electrode of said n channel MISFET;

(c) a step of depositing a first film on said semiconductor substrate, and removing said first film in the memory cell forming area;

(d) a step of depositing a second film on said semiconductor substrate;

(e) a step of performing an anisotropic etching relative to said first and second films in said peripheral circuit forming area, and thereby leaving the first and second films on a sidewall of the gate electrode in said peripheral circuit forming area; and

(f) a step of using said first and second films as a mask to implant an impurity into both sides of each of the gate electrodes of said n channel MISFET and said p channel MISFET and thereby form a semiconductor area.

11. The production method according to claim 10, further comprising a step of forming said capacitor connected to the memory cell selecting n channel MISFET, wherein said step of forming said capacitor includes a step of forming capacitors made of metal, for a lower electrode and an upper electrode thereof.

12. The production method according to claim 11, wherein metal composing one of said lower electrode

and said upper electrode is Ru.

13. The production method according to claim 1,

wherein the arrangement of said memory cell is an open bit line arrangement.

14. A semiconductor integrated circuit device comprising:

a memory cell composed of a memory cell selecting n channel MISFET and a capacitor which are formed in a memory cell forming area of a semiconductor substrate; and

an n channel MISFET and a p channel MISFET which are formed in peripheral circuit forming areas,

wherein each of said n channel MISFET and said p channel MISFET includes: a source and drain formed in said semiconductor substrate; a gate electrode formed between said source and drain on the semiconductor substrate via a gate insulating film; and an insulating film formed on said gate electrode,

said memory cell selecting n channel MISFET includes: a source and drain formed in said semiconductor substrate; a gate electrode formed between said source and drain on the semiconductor substrate via a gate insulating film; an insulating film formed on said gate electrode; and a film formed on a sidewall of the gate electrode of said memory cell selecting n channel MISFET,

a p type impurity is contained in the gate electrode of said memory cell selecting n channel MISFET and in the gate electrode of said p channel MISFET, and an n type

impurity is contained in the gate electrode of said n channel MISFET, and

the source and drain of each of said n channel MISFET and said p channel MISFET is formed with using, as a mask, a film thicker than a film formed on the sidewall of the gate electrode of said memory cell selecting n channel MISFET.

15. The semiconductor integrated circuit device according to claim 14,

wherein a conductive film is formed between the films formed on the sidewalls of said gate electrode and a gate electrode adjacent thereto in said memory cell forming area and is formed on said source and drain.

16. The semiconductor integrated circuit device according to claim 14,

wherein each of said insulating film formed on said gate electrode and the film formed on the sidewall of the gate electrode of said memory cell selecting n channel MISFET is a film containing one of no hydrogen and little hydrogen.

17. The semiconductor integrated circuit device according to claim 15,

wherein the film formed on the sidewall of the gate electrode of said memory cell selecting n channel MISFET is a silicon oxide film, and said conductive film is a silicon film.

18. The semiconductor integrated circuit device

according to claim 14,

wherein said capacitor includes a lower electrode and an upper electrode which are made of metal, and a capacitor insulating film.

19. The semiconductor integrated circuit device according to claim 18,

wherein metal composing one of said lower electrode and said upper electrode is Ru.

20. The semiconductor integrated circuit device according to claim 14,

wherein the arrangement of said memory cell is an open bit line arrangement.

21. A semiconductor integrated circuit device having a memory cell composed of a memory cell selecting n channel MISFET and a capacitor, said semiconductor integrated circuit device comprising:

a source and drain formed in a semiconductor substrate;

a gate electrode formed between said source and drain on the semiconductor substrate through a gate insulating film, the gate electrode containing a p type impurity; and

a first film formed on said gate electrode and a second film formed on a sidewall of said gate electrode,

wherein each of said first and second films is a film containing one of no hydrogen and little hydrogen.

22. The semiconductor integrated circuit device according to claim 21,

wherein a conductive film is formed between the films formed on the sidewalls of said gate electrodes and a gate electrode adjacent thereto and is formed on said source and drain.